REMARKS

Claims 1-25 are pending in the application. Claims 1, 2 and 4-25 are allowed.

Claim 3 is amended herein to clarify the present invention. The signal line of the amended claim 3 is directly connected with the main memory.

Claim 3 is rejected under 35 U.S.C. § 102(b) as being anticipated by Iwasa et al. (U.S. 5,522,058) (Iwasa).

In the Office Action it is asserted that a sharing indication line 18 of Iwasa corresponds to a signal line of applicant's claim 3 and a cache memory control section of claim 3 is taught by the Iwasa disclosure at column 36, lines 10-30. Applicant respectfully disagrees for at least the following reasons:

Applicant's specification describes an address line 20 and a data line 22 of the internal bus are directly connected with main memory and the cache control unit 17. In contrast Iwasa describes a sharing indication line 18 is not directly connected with the main memory. Applicant's claim 3 is clarified to recite, in contrast to Iwasa, the signal line is directly connected with the main memory.

The cache memory control section of claim 3 outputs directly, data and an address of the cache memory, to the signal line in accordance with the command inputted over the second bus. Applicant's claimed invention provides advantages over the cited reference in that the cache memory control section can perform write back processing into the main memory directly through the signal line even if the first bus is locked and the write back processing into the main memory can not be performed through the first bus.

Iwasa is in contrast to the claimed invention because as shown in fig. 37 of Iwasa, when write back processing into the main memory M0 is performed, the data of the cache memory C1 is transmitted to the shared bus SB. Therefore, when the shared bus SB is locked, the data of the cache memory C1 cannot be transmitted to the sharing management unit S0.

As shown in fig. 4 of Iwasa, the cache control unit 17 and the main memory 3 are connected to the internal bus 5, but the cache control unit 17 and the main memory 3 are not directly connected the other signal line which is different from the internal bus 5 for outputting data and an address of a cache data memory unit 13 when the internal bus 5 is locked.

As described in column 10, lines 57-60 of Iwasa, the sharing indication line 18 is a line for transmitting a signal indicative of whether the address to be accessed is shared by the cache memory on the other processor board or not, the sharing indication line 18 is not one for outputting data and an address of the cache data memory unit 13 when the internal bus 5 is locked. Therefore, the sharing indication line 18 of Iwasa is quite different from the signal line of claim 3.

As shown in fig. 15 of Iwasa, the cache control unit 17 reads data from the main memory 3 through the address line 19, and the data line 22 of the internal bus 5. As shown in fig. 37 and described in column 36, lines 43-46, of Iwasa, the newest value transmitted through the shared bus SB is written into a main memory M0 through the address line 19, and the data line 22 the internal bus 5 which corresponds to the first bus which is different from the signal line of claim 3.

In contrast to applicant's claimed invention in Iwasa the address line 19, and the data line 22 of the internal bus 5 are shared in read processing of data from the main memory 3 and the write back processing into the main memory 3. Therefore, when the internal bus 5 is locked

during read processing by bus failure, write back processing into the main memory 3 can not be performed.

Further, Iwasa do not teach or suggest the signal line which is directly connected with the main memory and the cache memory control section for outputting data and an address of the cache memory when the first bus is locked and the cache memory control section for outputting data and an address of the cache memory to the signal line of claim 3.

The sharing indication line 18 of Iwasa is provided for transmitting a signal indicative of whether or not the address to be accessed is shared by the cache memory on the processor board.

With regard to the cache memory control section of applicant's claim 3, Iwasa disclose two lines connected with a main memory 3 and a cache 2 in Fig. 2. One of the lines is an internal bus 5 connected with the main memory 3, the sharing management unit 4, and the cache 2, the other is a bus line connected only with the cache 2 and the main memory 3.

In contrast to the disclosure in Iwasa, applicant's claim 3 provides that the first bus and the signal line are connected with the main memory and the cache control unit. The first bus is provided for reading data from the main memory and writing data into the main memory by the cache control unit of claim 3 when the write back command is not outputted to a second bus. The signal line is provided for writing back data into the main memory by the cache control unit when the write back command is outputted to the second bus, and data can be written into the main memory even if the first bus is kept locked.

For at least the foregoing reasons it is respectfully requested the rejection of applicant's claim 3 be withdrawn and the claim be placed in condition for allowance.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider

this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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